

Fig. 1: PRIOR ART

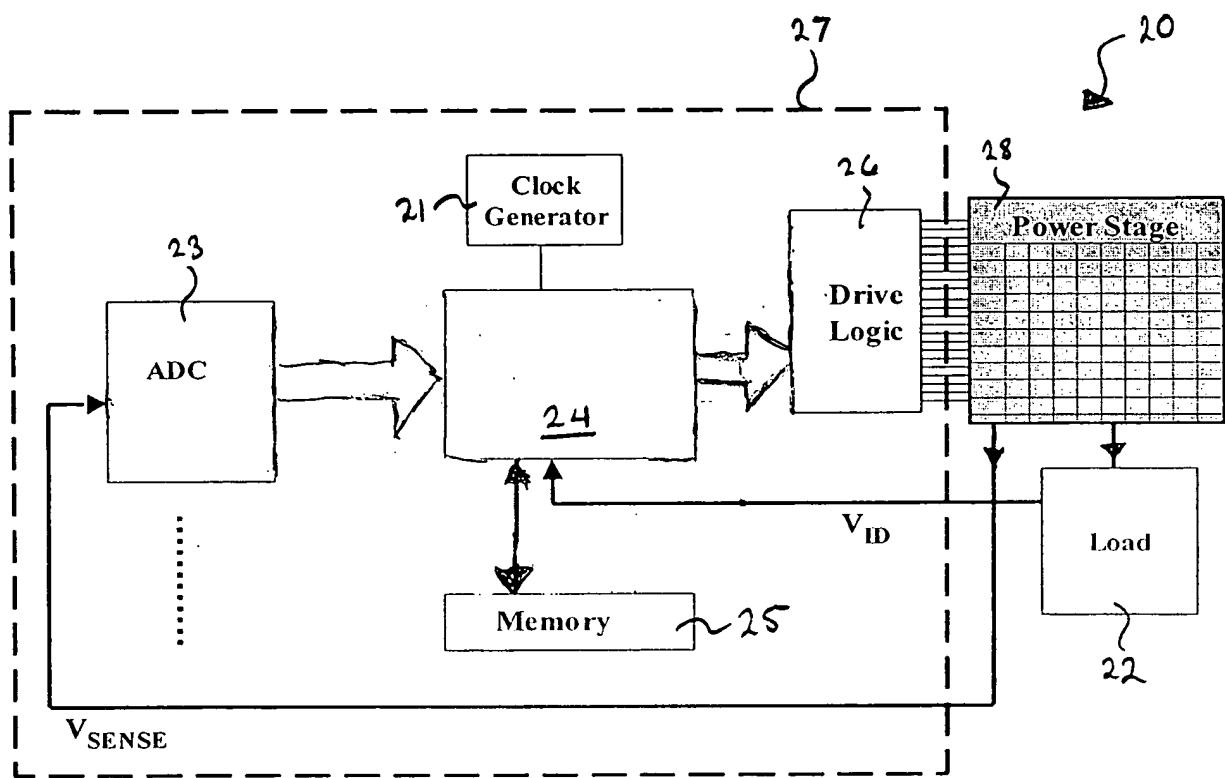


Fig. 2

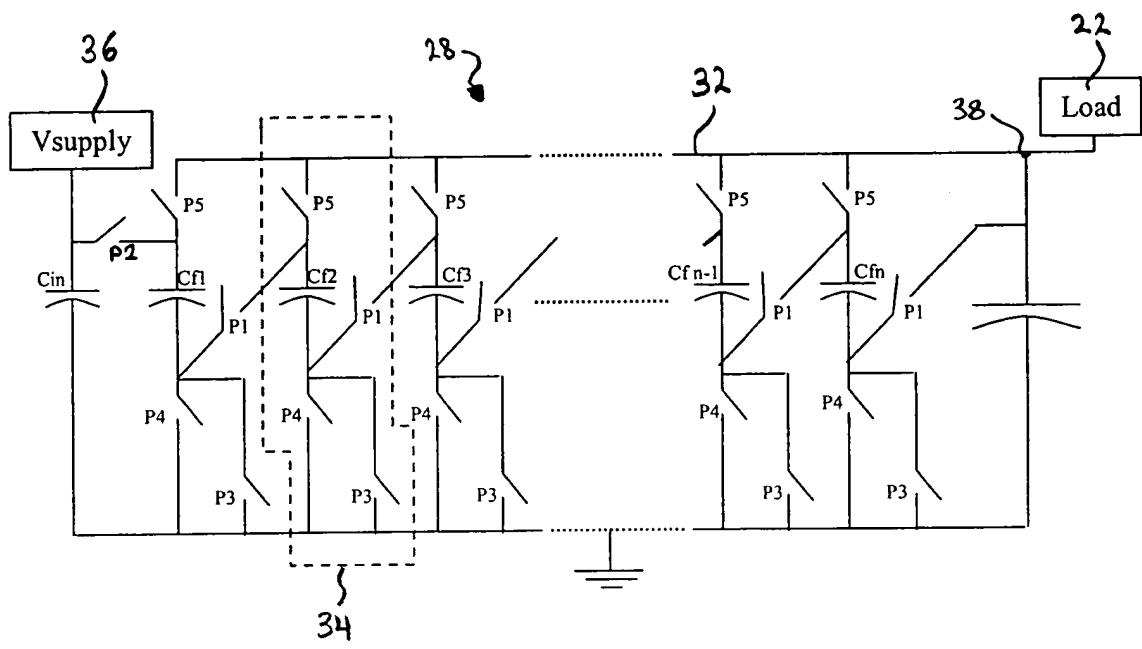


Fig. 3

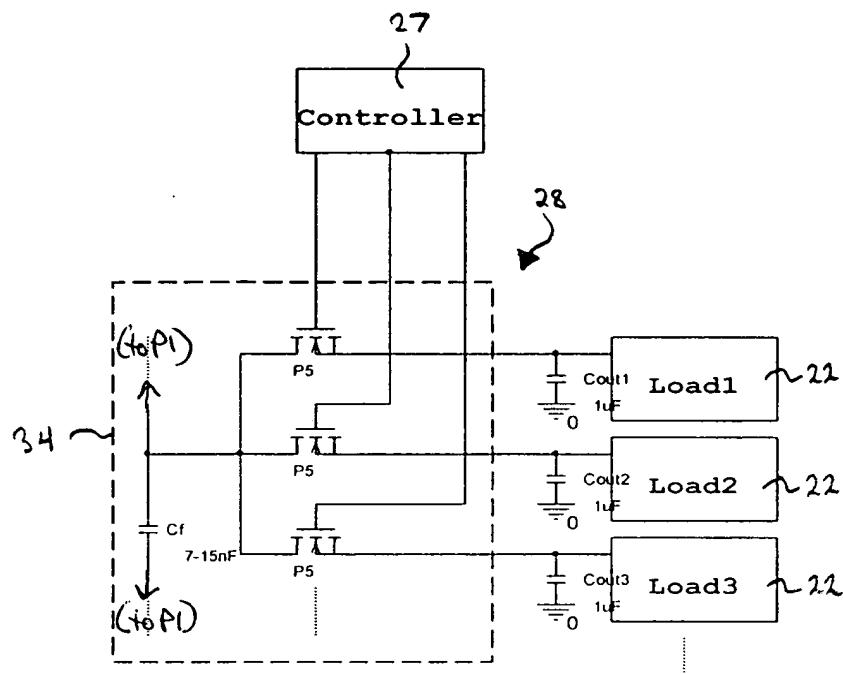


Fig. 4

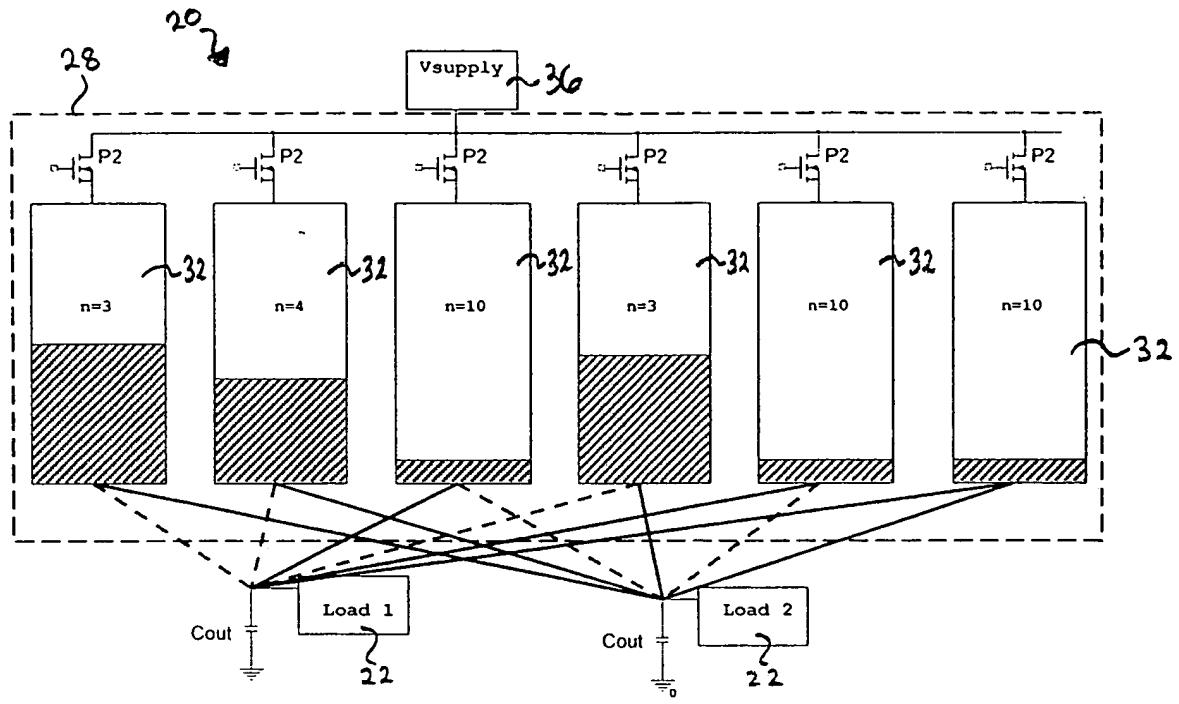


Fig. 5

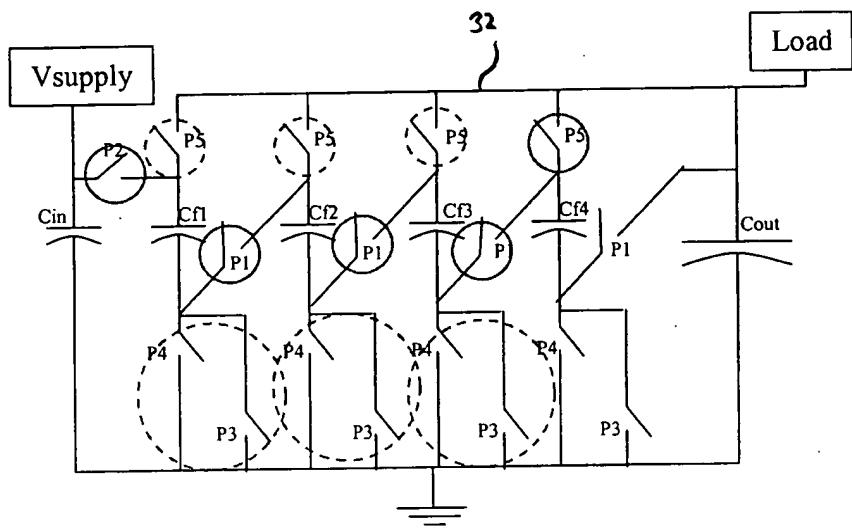


Fig. 6

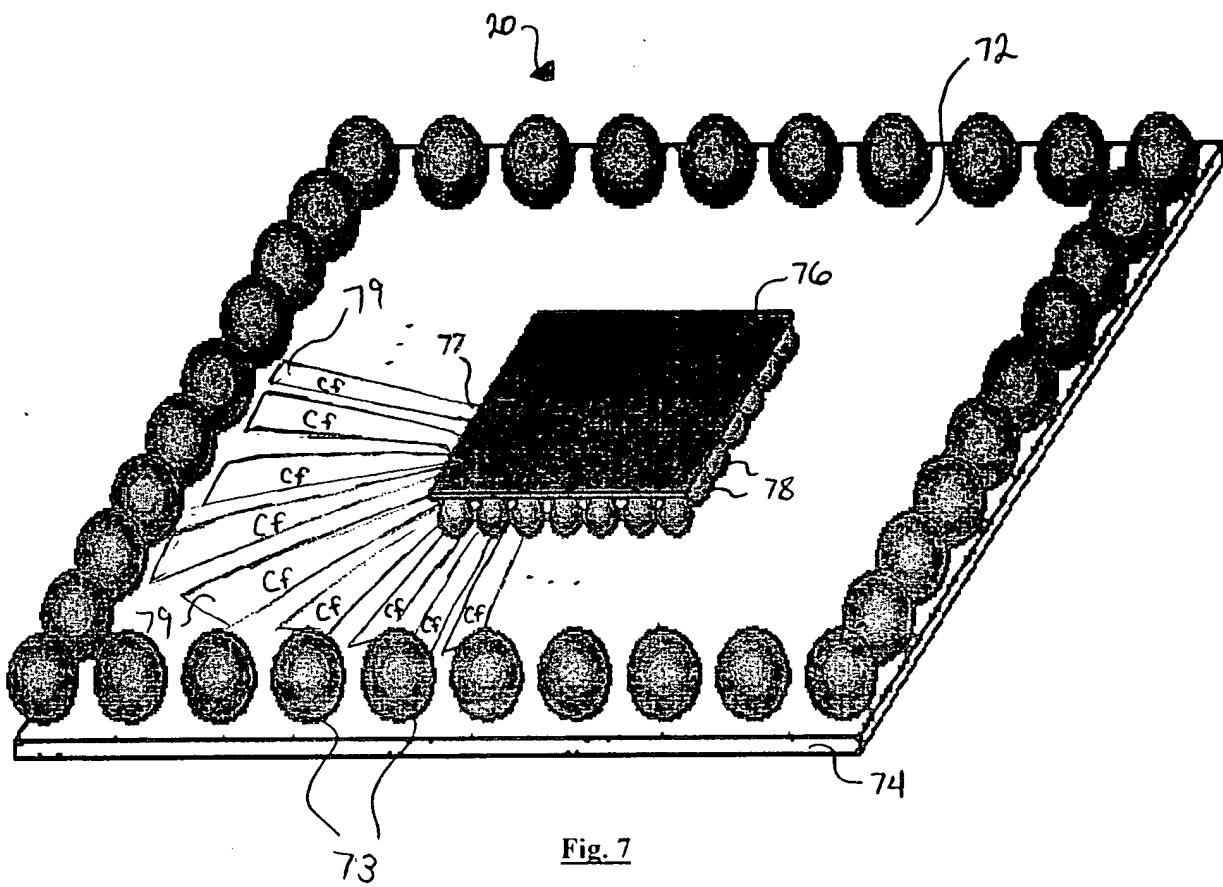


Fig. 7

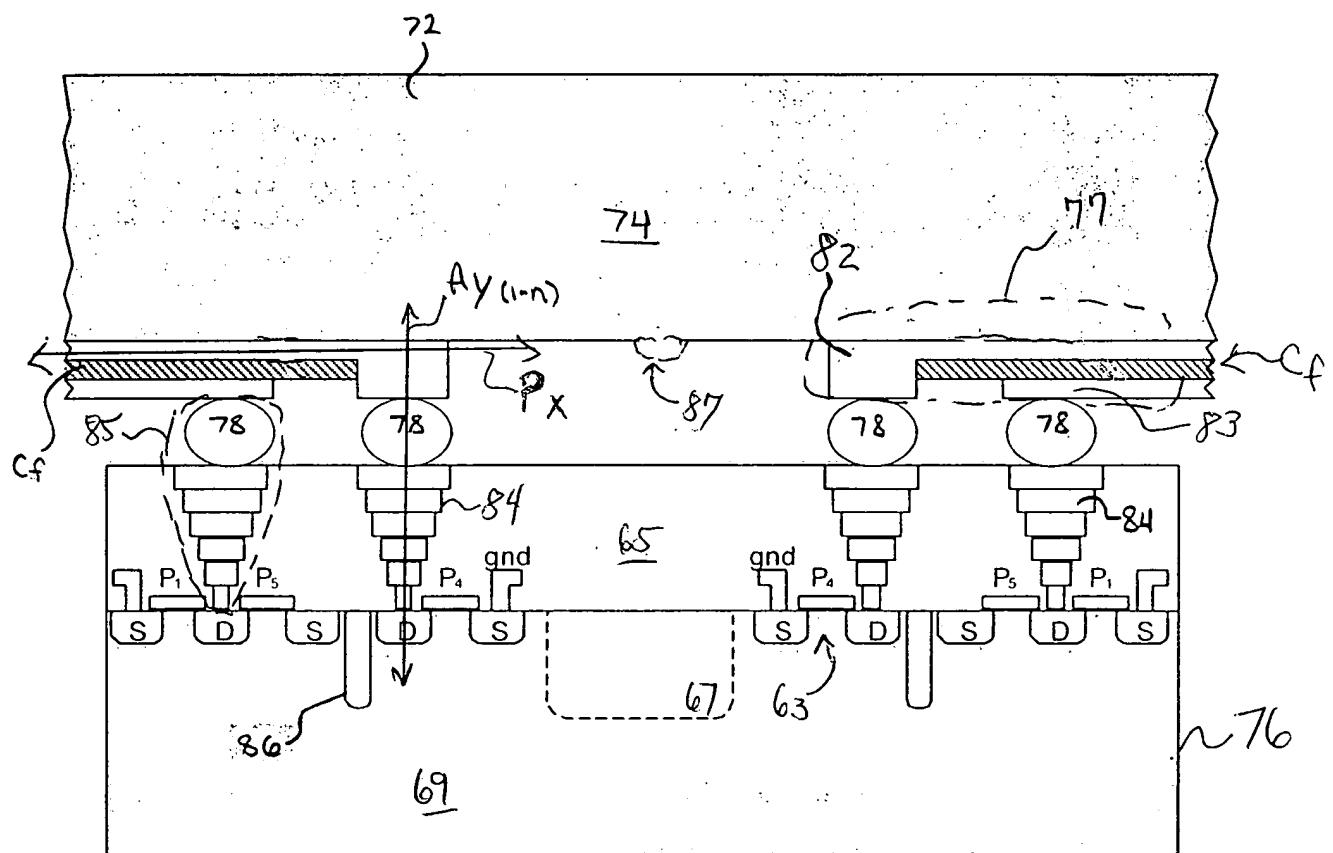


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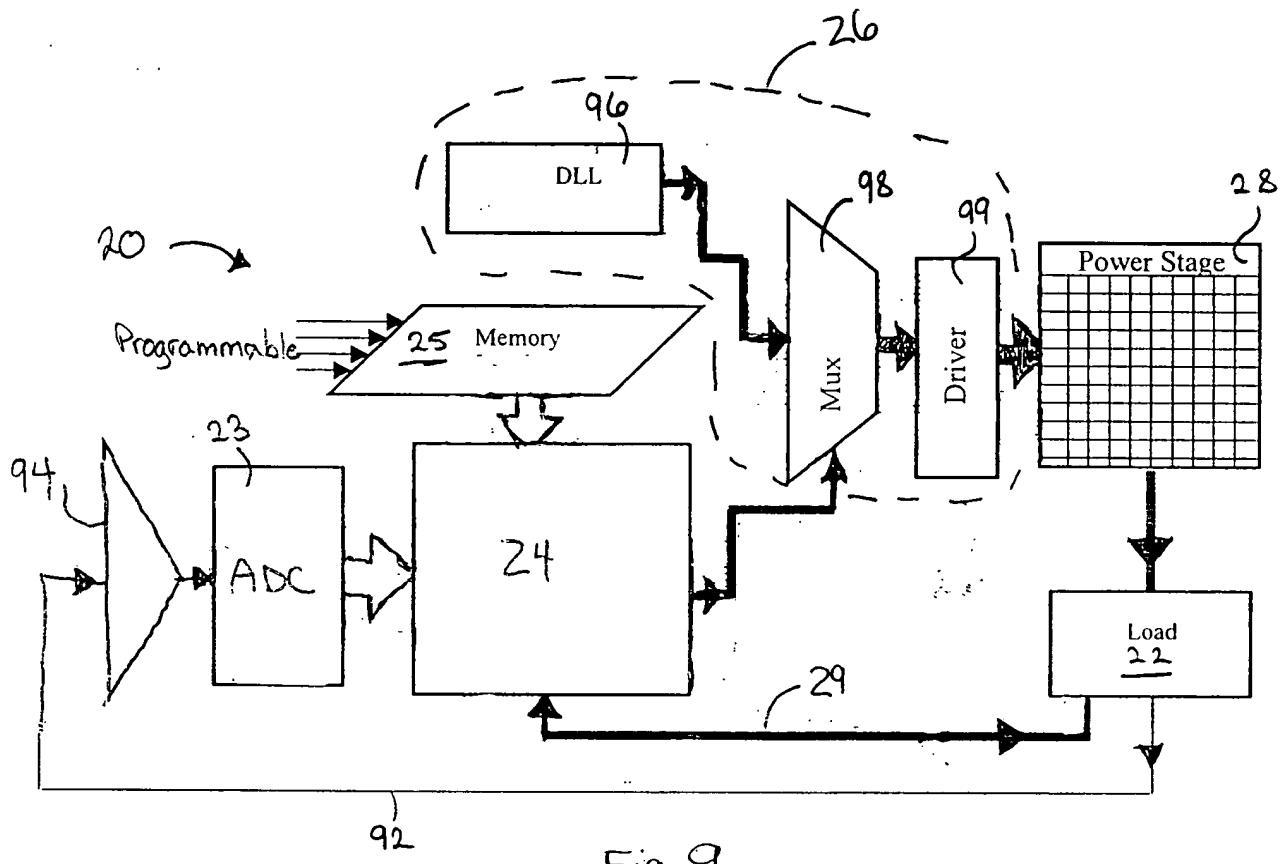


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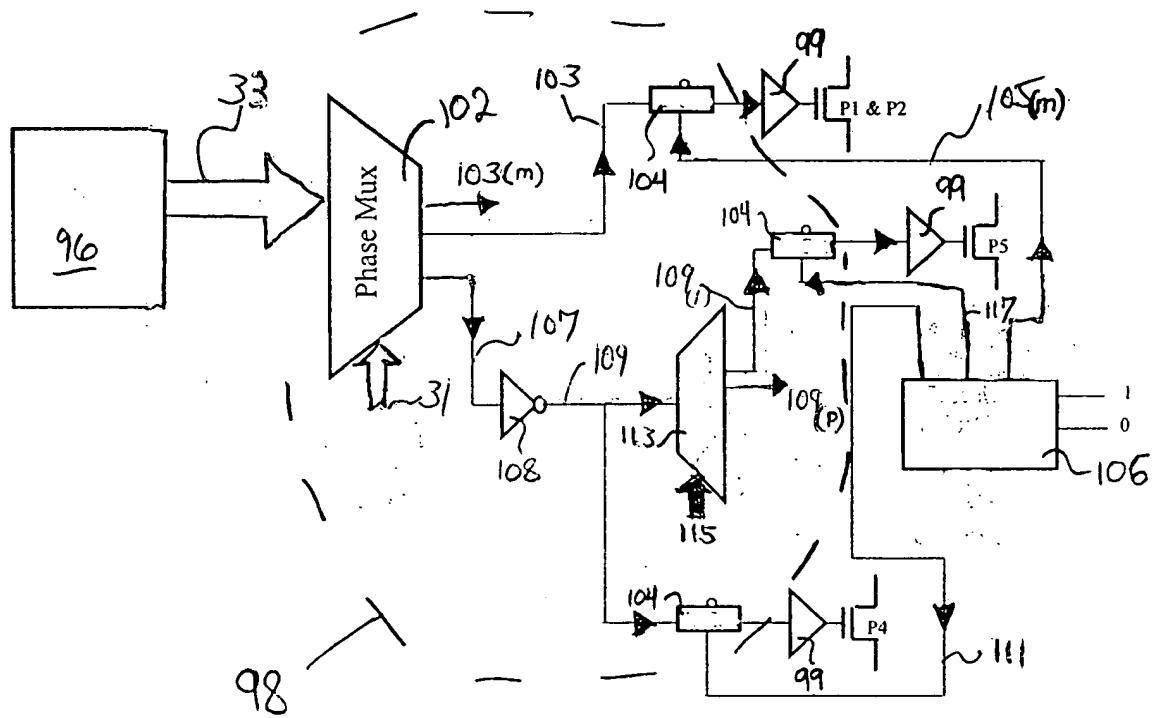


Fig. 10

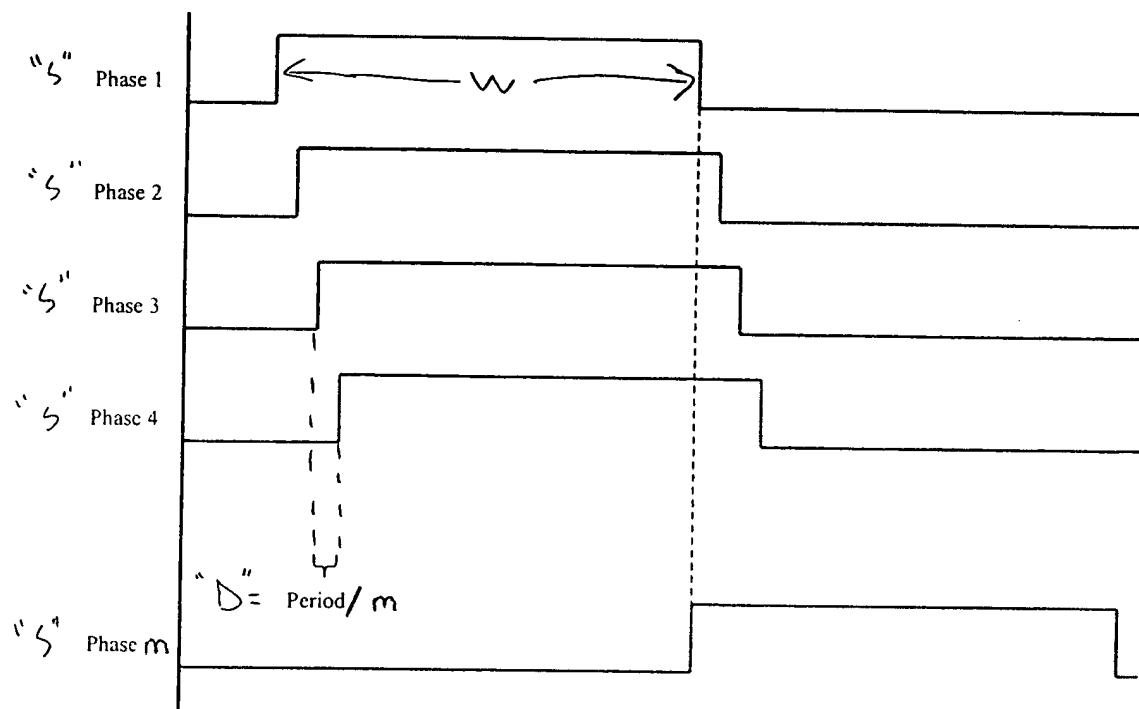


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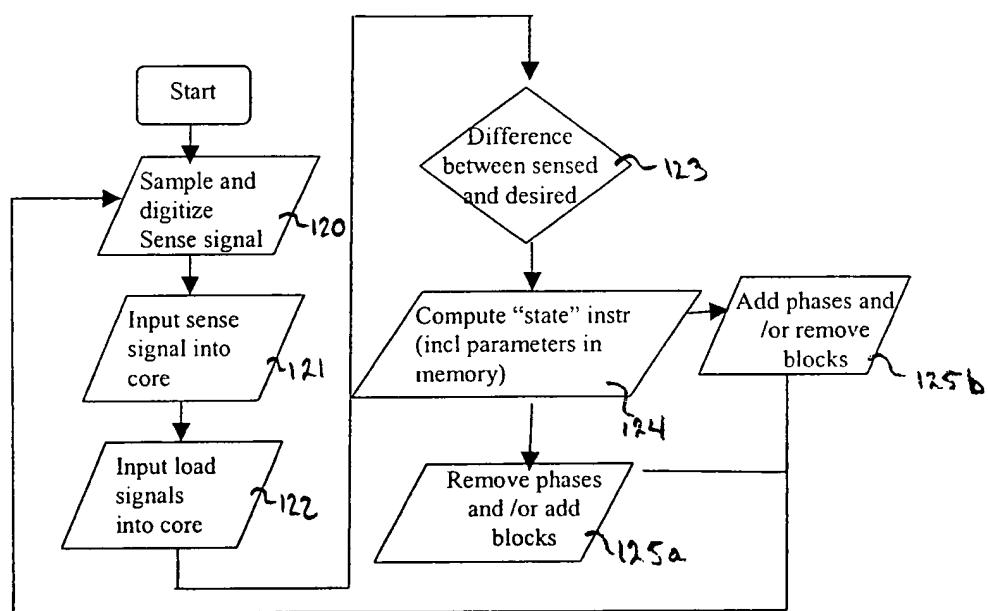


Fig. 12

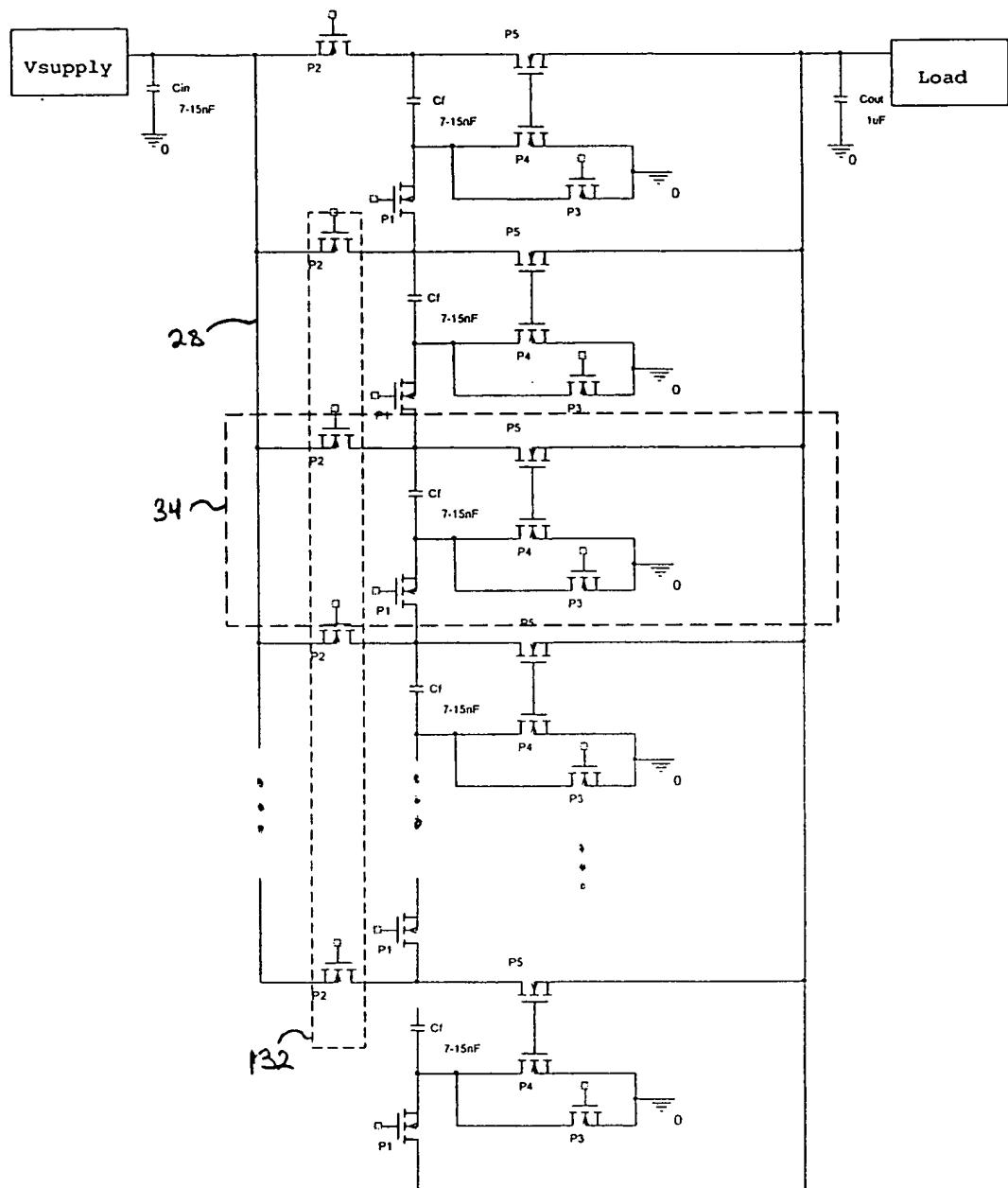


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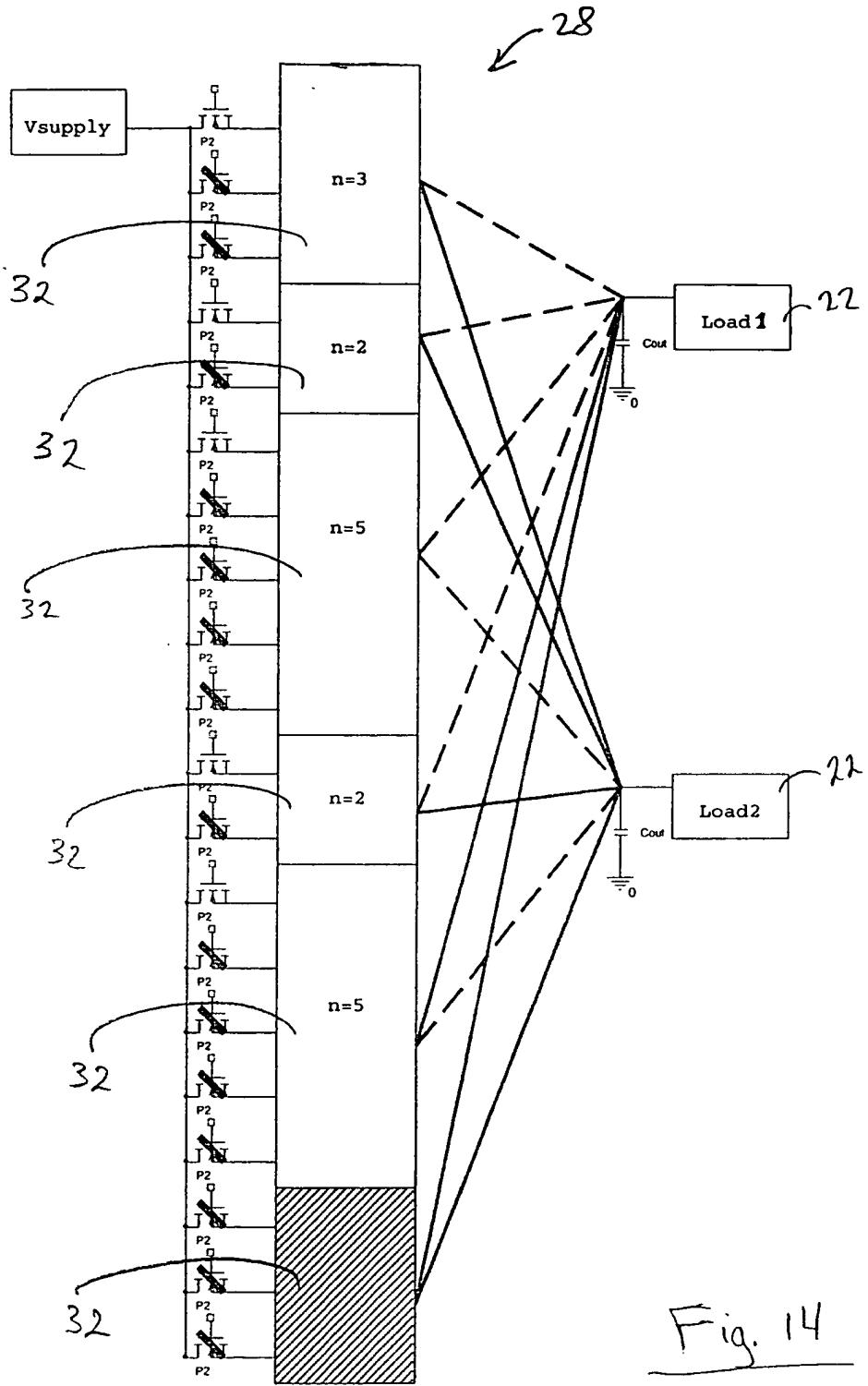


Fig. 14

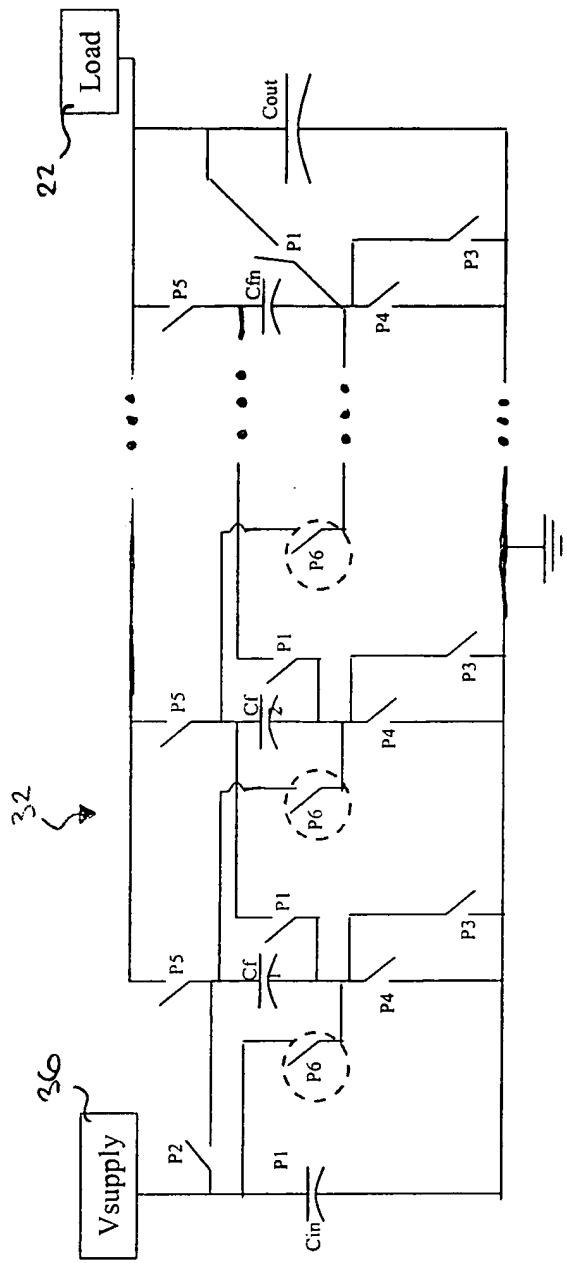


Fig. 15

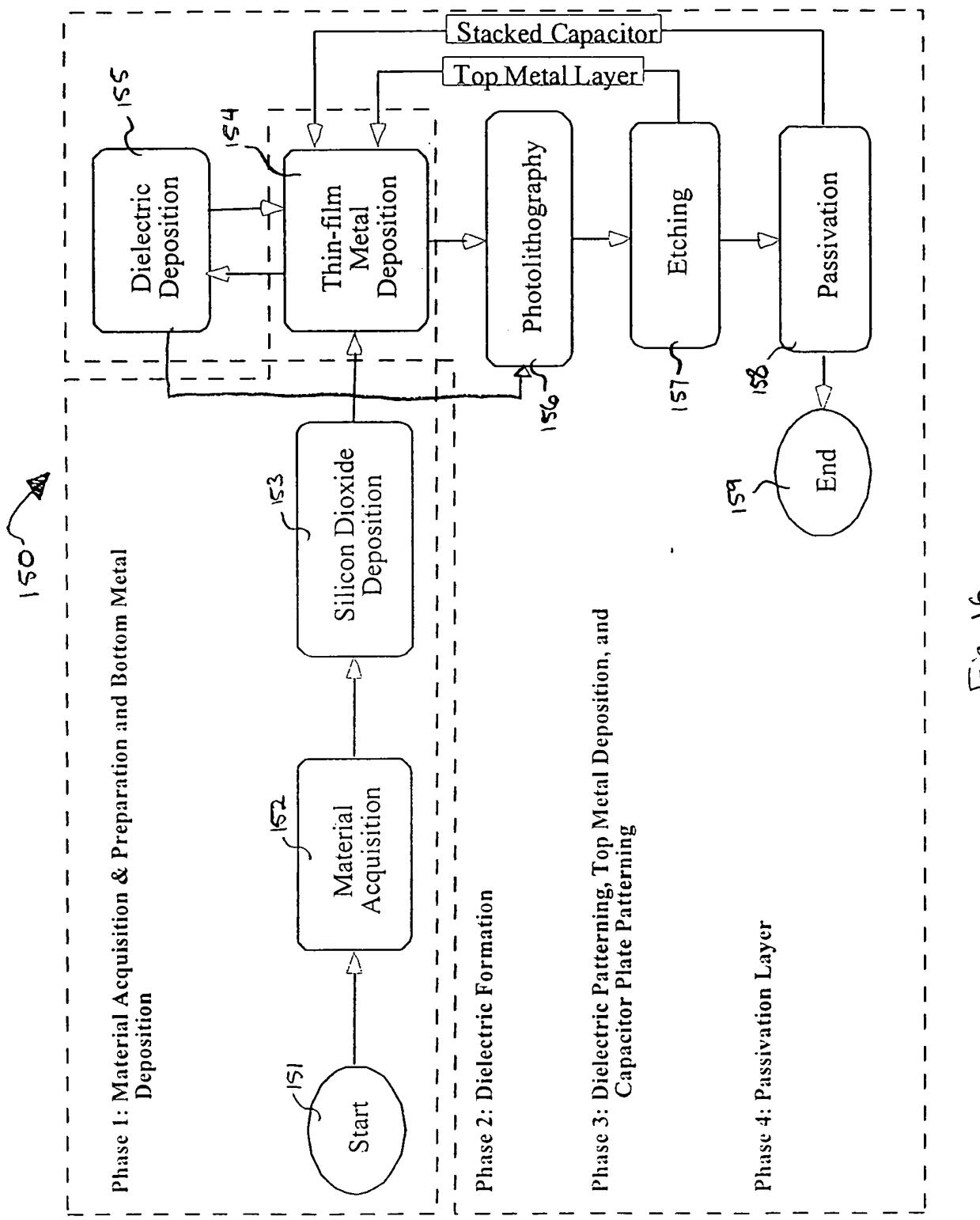


Fig. 16

PHASE	PROCESS STEPS	DESCRIPTION/NOTES	
1	MATERIAL ACQUISITION & PREPARATION		
	Obtain Silicon Wafer	1	Standard 8" Silicon (6"for prototype)
	Deposit SiO ₂	2	0.5-1.0 μm (insulation and adhesion)
	BOTTOM METAL DEPOSITION		
	Deposit Titanium	1	200 - 500 Å
	Deposit Copper	2	2 microns
	Deposit Tantalum	3	2000 Å
2	DIELECTRIC FORMATION		
	Tantalum Oxide Deposition	1	Anodization
3	DIELECTRIC PATTERNING	MASK 1	
	Apply Resist	1	Typically 4 microns
	Exposure	2	Minimum feature size: 20 microns
	Develop	3	
	Etch Tantalum Oxide	4	Typically RIE
	Etch Tantalum	5	Typically RIE
	TOP METAL DEPOSITION		
	Deposit Titanium	1	200 - 500 Å
	Deposit Copper	2	2 microns
	TOP METAL PATTERNING		MASK 2
4	Apply Resist	1	Typically 4 microns
	Exposure	2	Minimum feature size: 20 microns
	Develop	3	
	Etch Copper	4	Wet or dry
	Etch Titanium	5	Wet or dry
	Strip Resist	6	
	PASSIVATION (OPTIONAL)		
	Apply BCB	1	
	Exposure	2	
	Develop	3	
	Cure	4	

Fig. 17

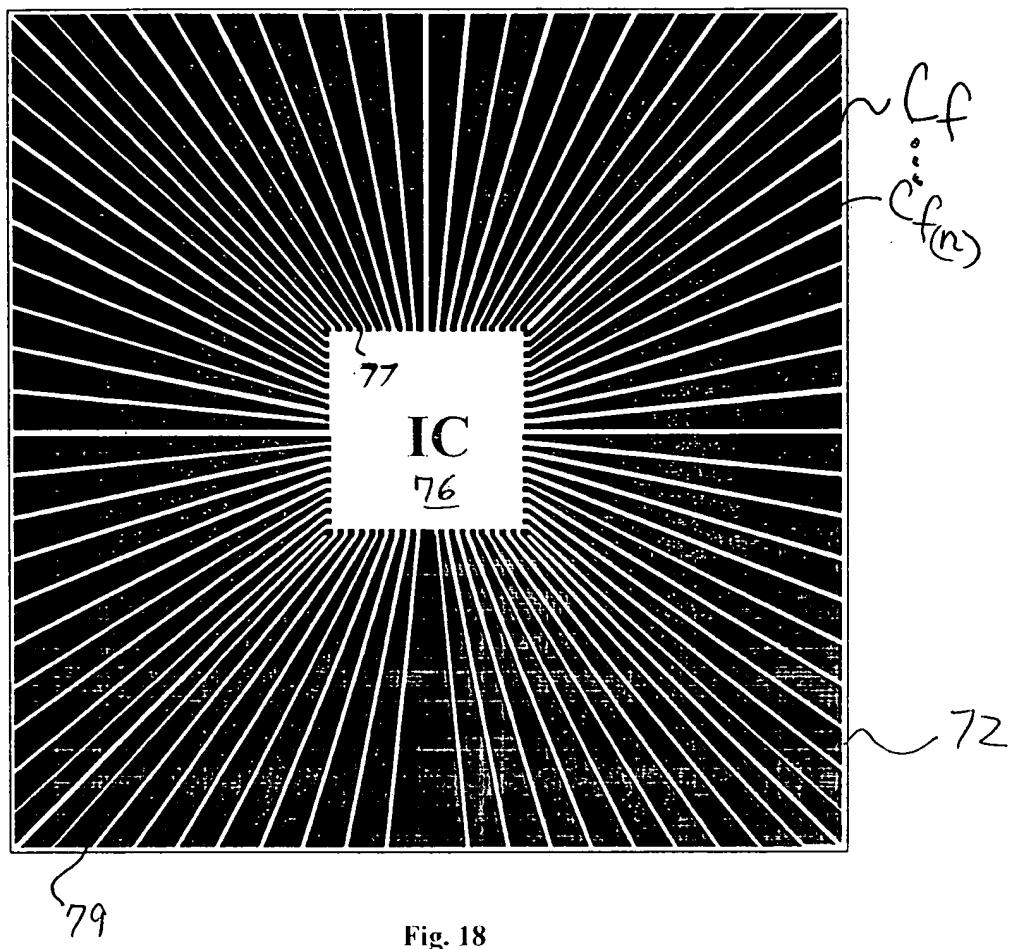


Fig. 18

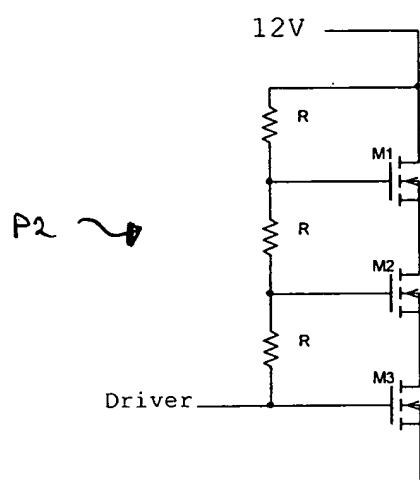


Fig. 19

Input Voltage	Gate Length (Process)	Qg (pC)	Fsw (MHz)
12	0.8 um	>40	1-5
12	0.5 um	27	10-20
5	0.5 um	27	10-20
5	0.35 um	20	20-30
3.3	0.35 um	20	20-30
3.3	0.25 um	10	50-60
3.3	0.18 um	6	80-100

Fig. 20

Transient Up Response

1 A/ns transient. 6 ns [166 MHz] delay to model controller sampling and response

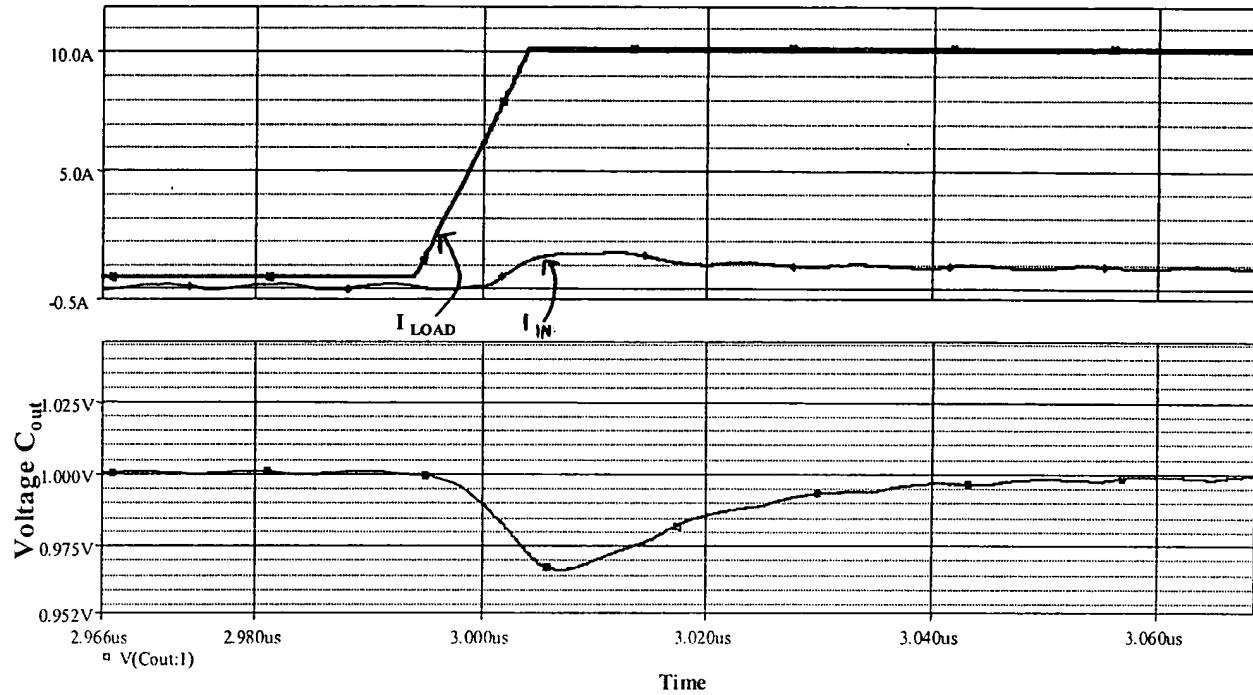


Fig. 21

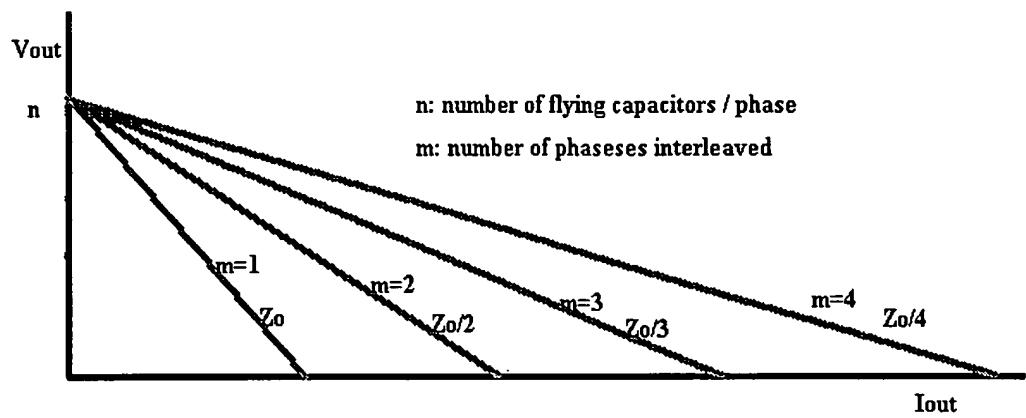


Fig. 22

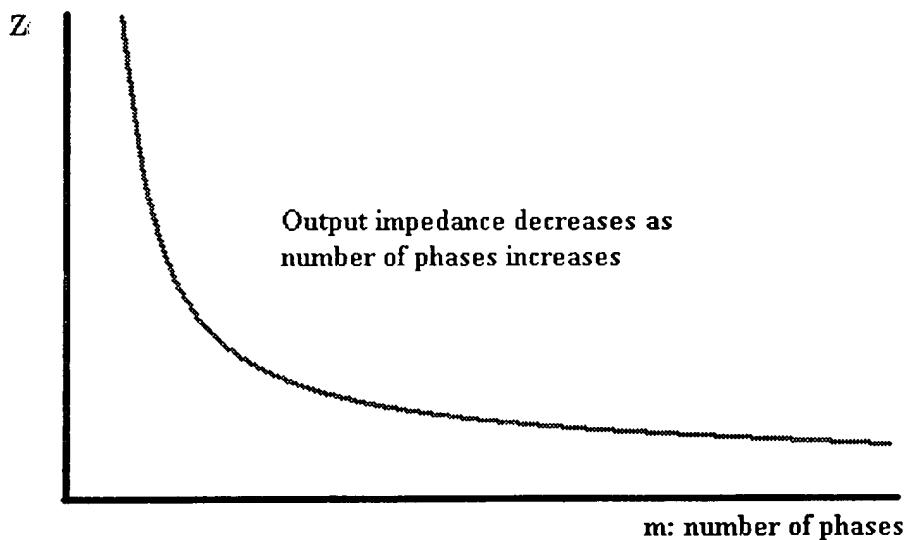


Fig. 23

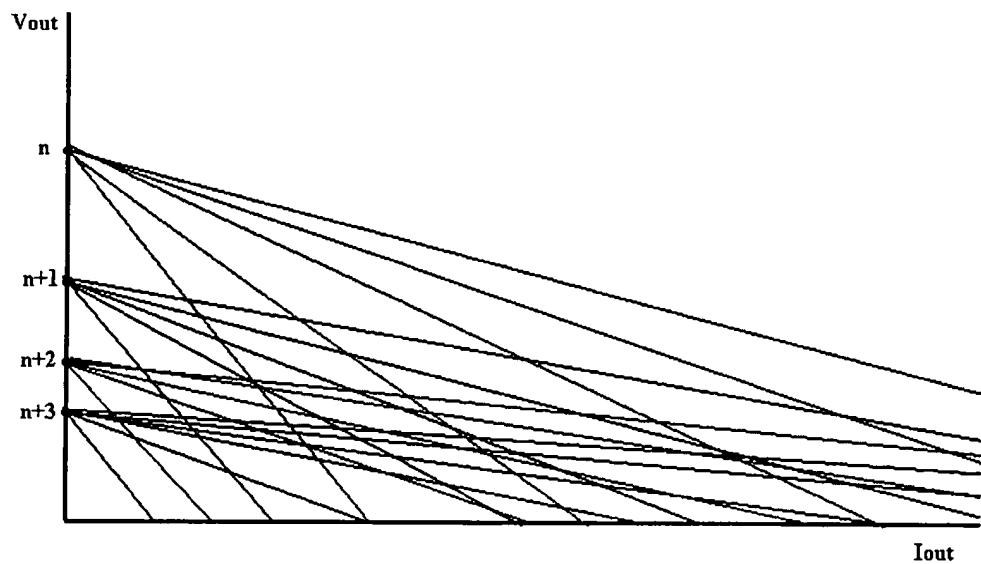


Fig. 24

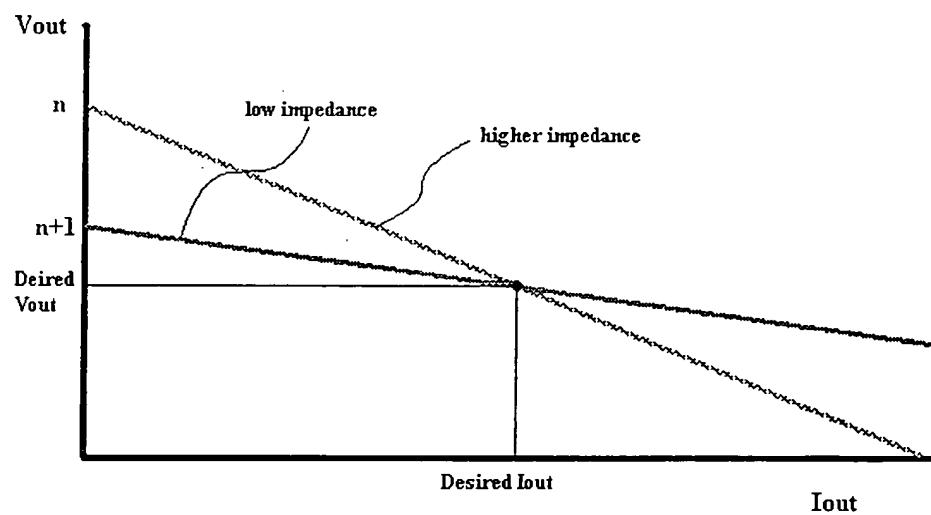


Fig. 25

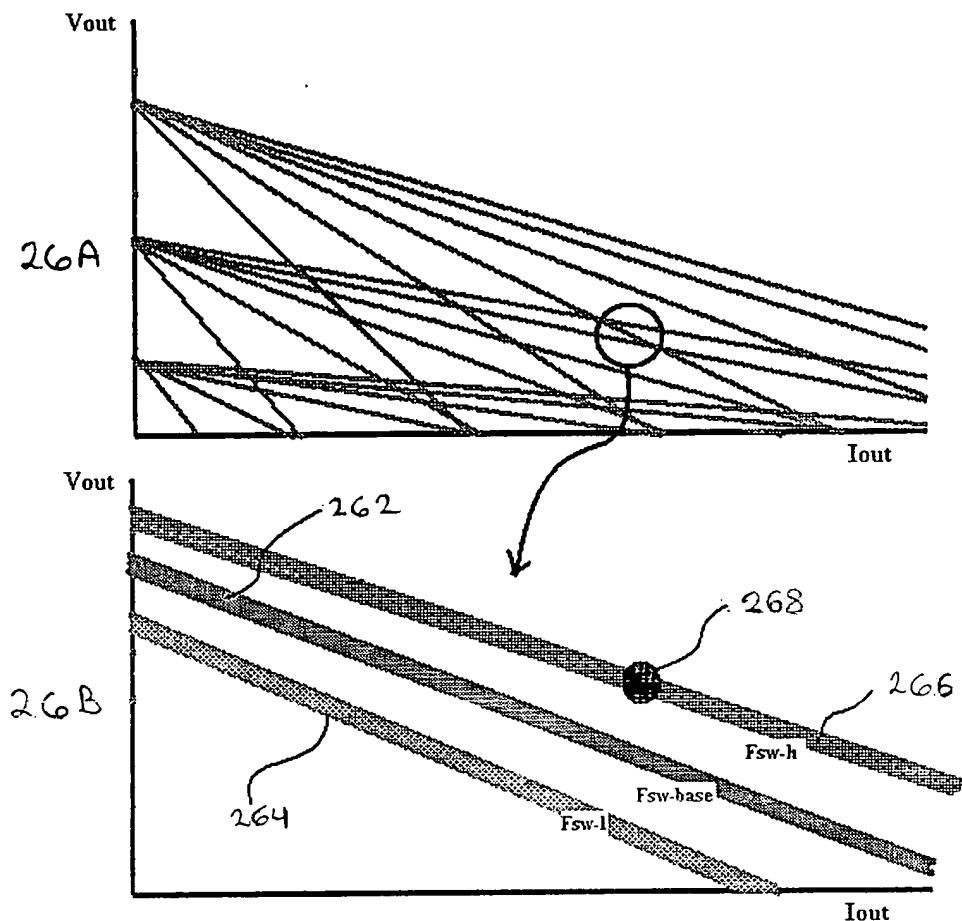


Fig. 26

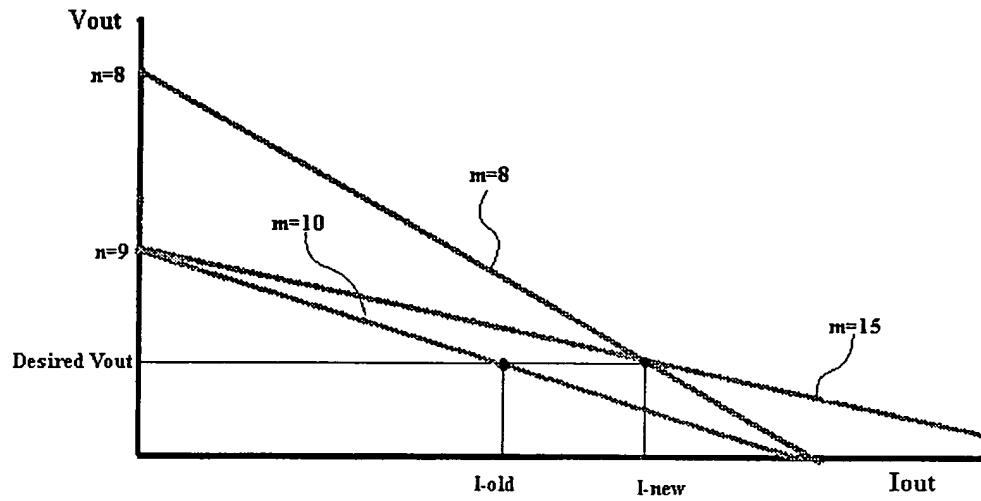


Fig. 27

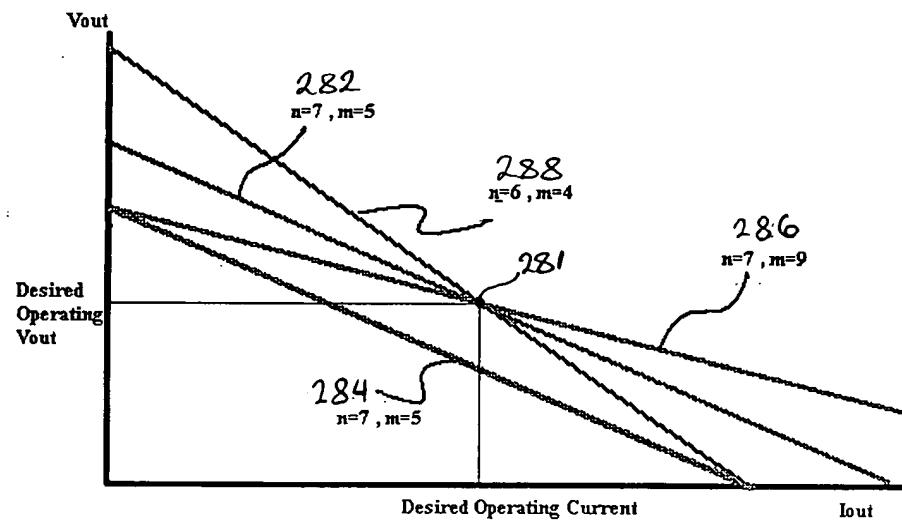


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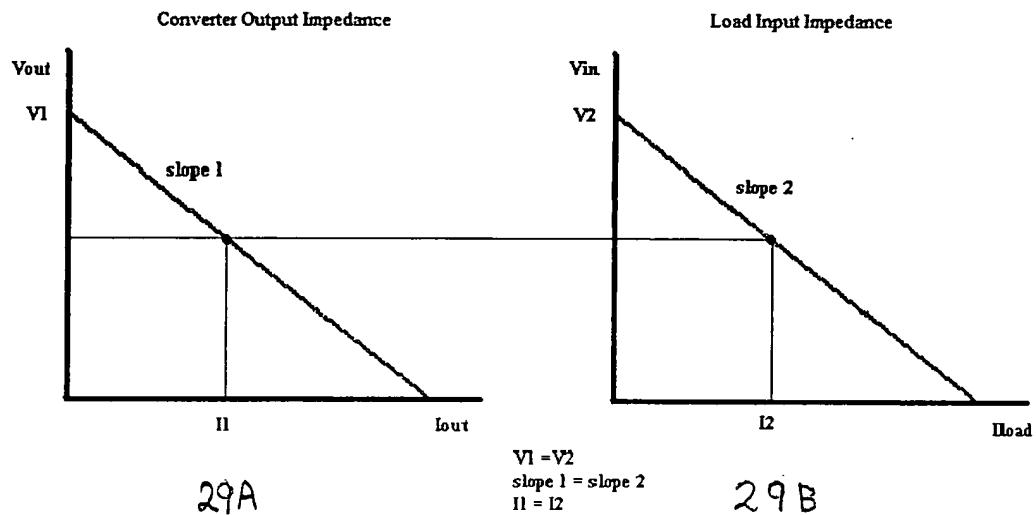


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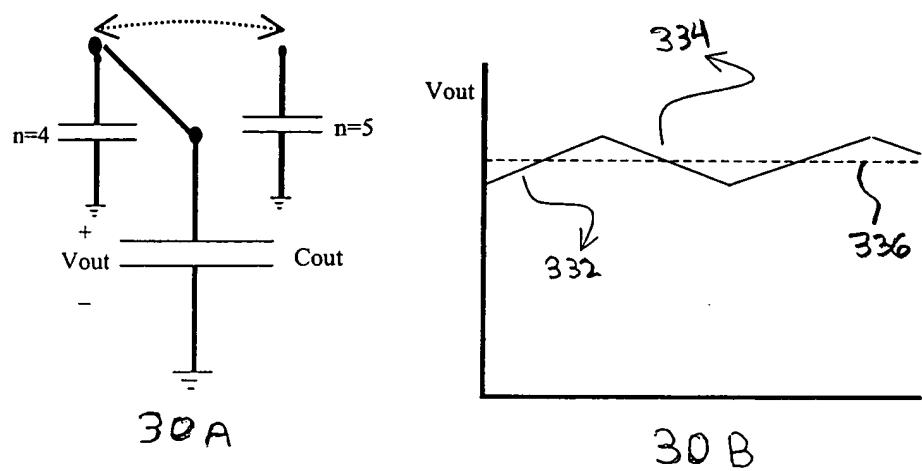
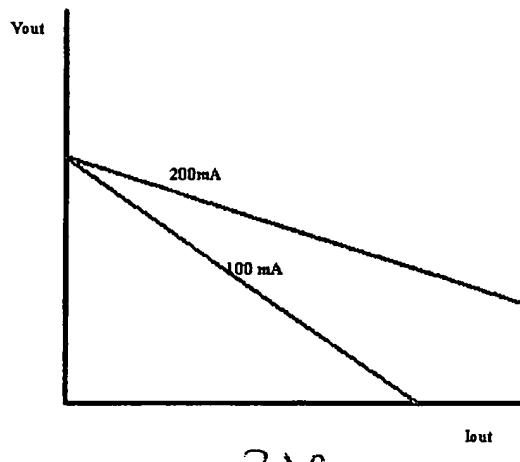
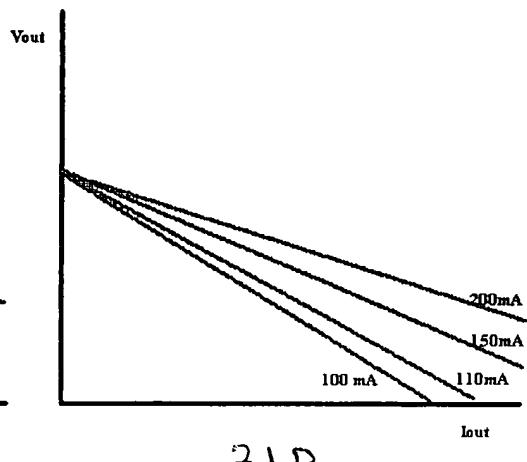


Fig. 30



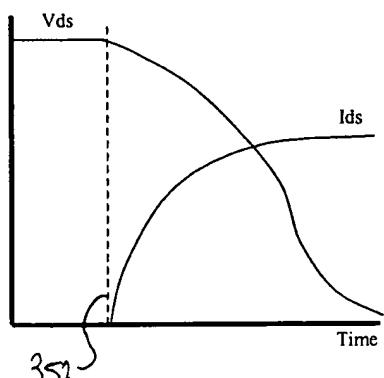
31A



31B

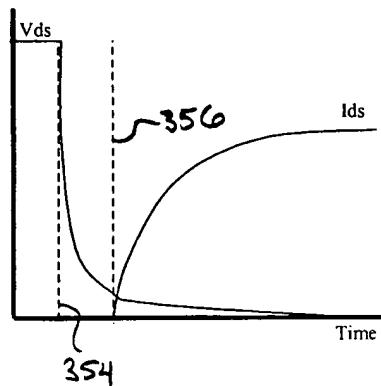
Fig. 31

P2, P4, P5 w/o LVS



32A

P2, P4, P5 w/ LVS



32B

Fig. 32

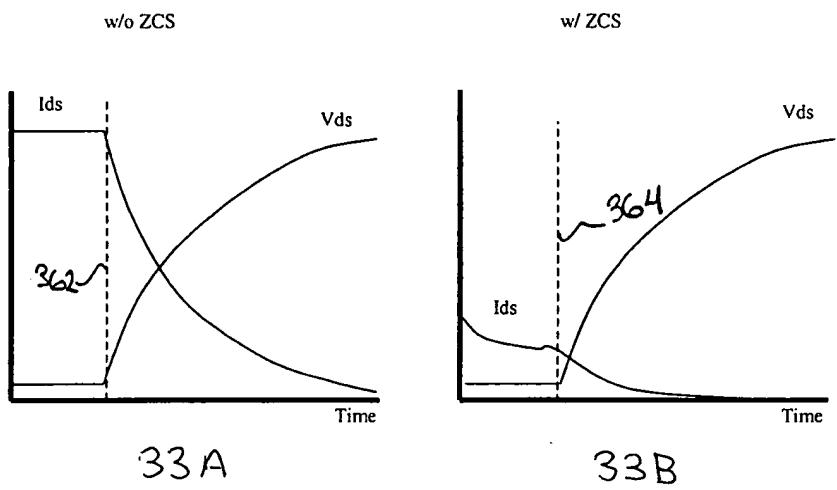


Fig. 33

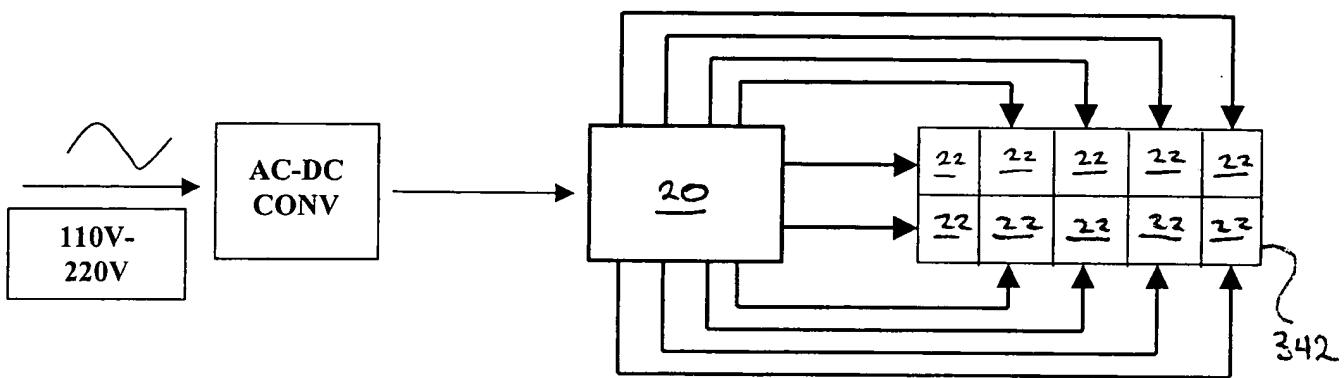


Fig. 34

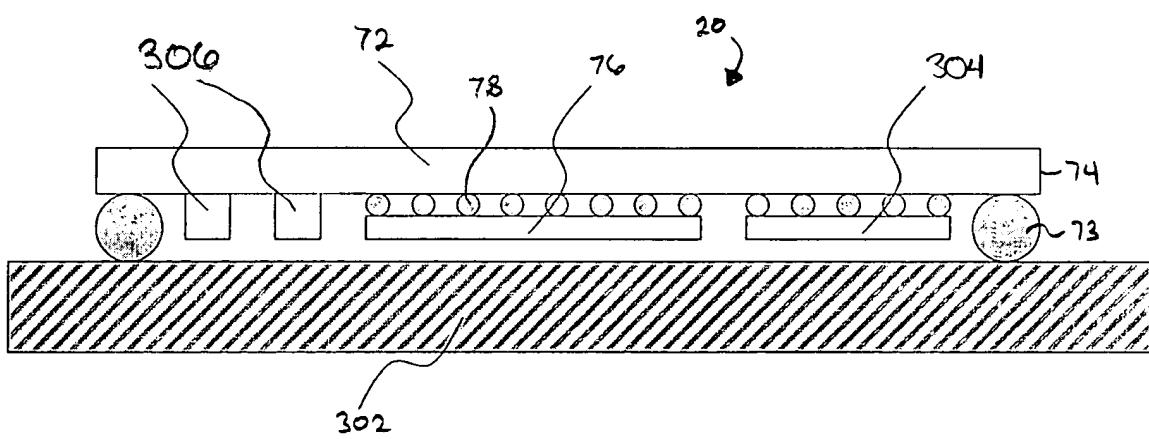


Fig. 35

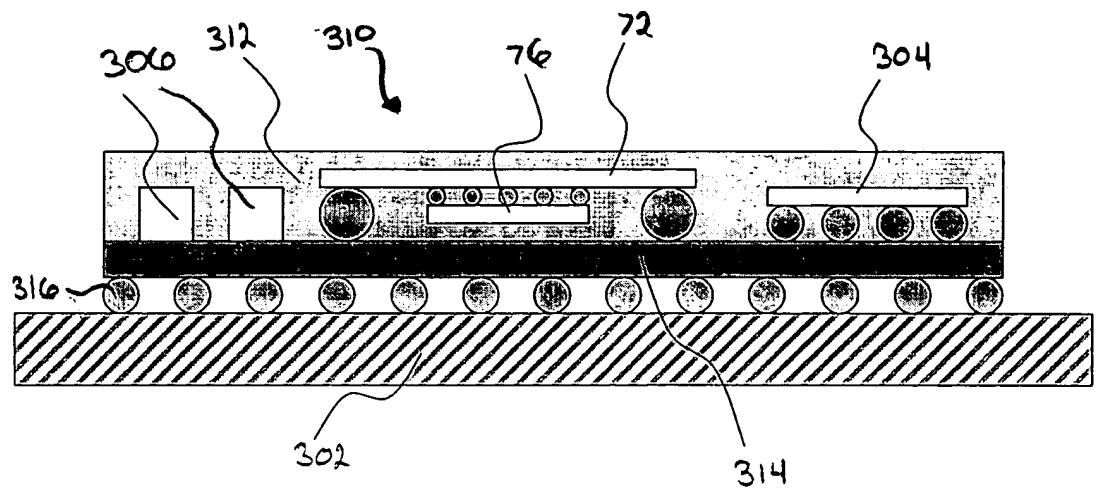


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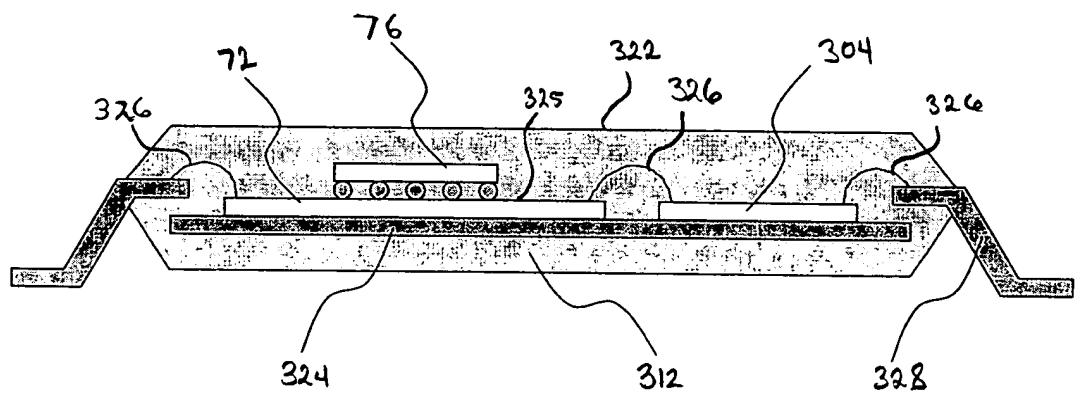


Fig. 37

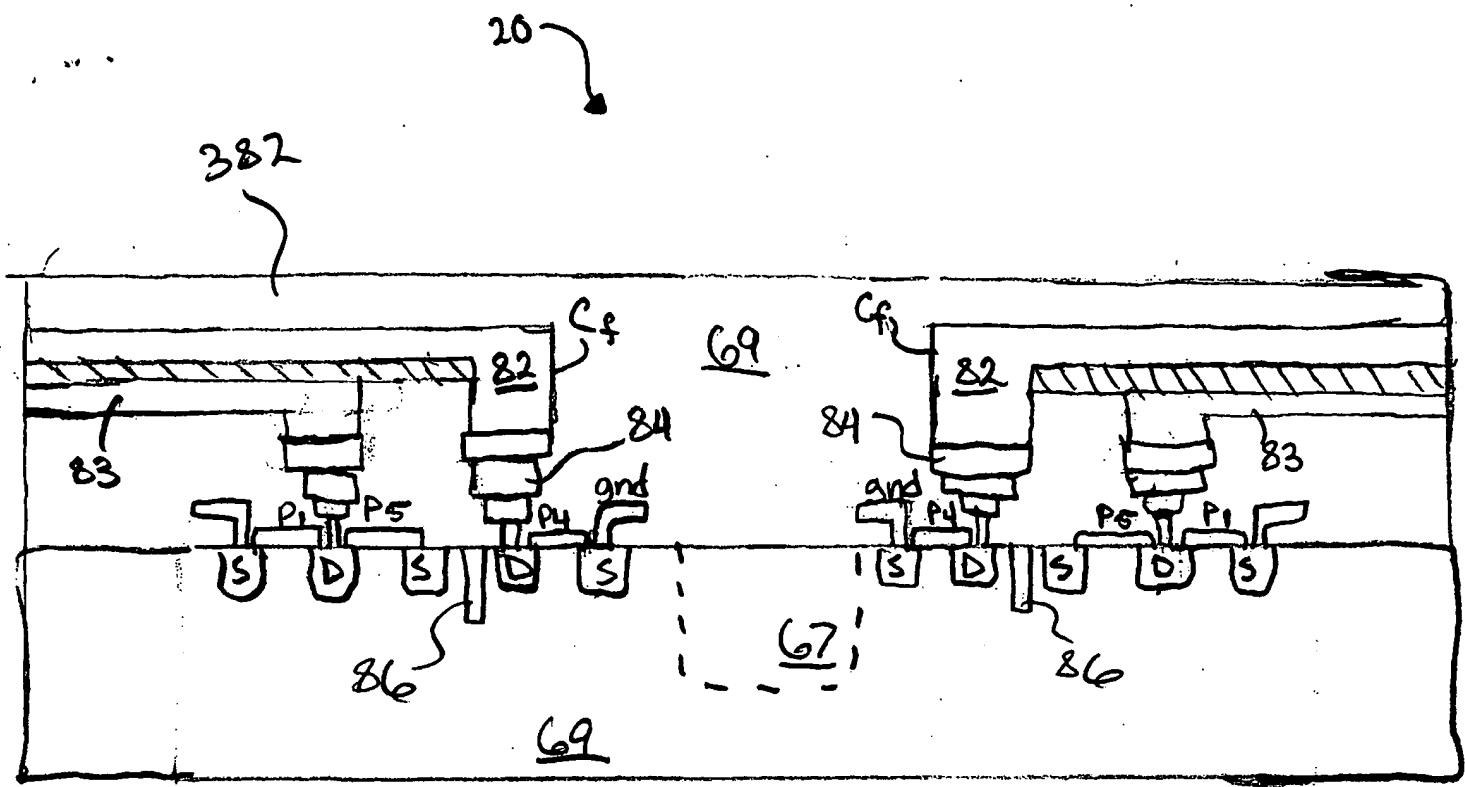


Fig. 38